

| Teaching Scheme | | Examination Scheme | | | | |
|-----------------|----------------|--------------------|--------------|--------------------|-----------------|-------------|
| Theory Hrs. | Practical Hrs. | Theory Hrs. | Theory Marks | Pract./ Viva Marks | Term Work Marks | Total Marks |
| -- | 2 | -- | -- | -- | 50 | 50 |

SYLLABUS

1. **Fabrication of MOSFET:** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.
 2. **MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure & Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling & small-geometry effects, MOSFET capacitances
 3. **MOS inverters: Static characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load), CMOS Inverter
 4. **MOS inverters Switching characteristics and Interconnect Effects:** Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters
 5. **Combinational MOS Logic circuits:** Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs)
 6. **Sequential MOS Logic circuits:** Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch & Flip-flop circuit, CMOS D-latch & Edge-triggered flip-flop
 7. **Dynamic Logic Circuits:** Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits
 8. **Chip I/P and O/P circuits:** On chip Clock Generation and Distribution, Latch –Up and its Prevention
 9. **Design for testability:** Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self Test (BIST) techniques, current monitoring IDDQ test
 10. **VHDL Programming:** Data Flow & Structural Modeling using VHDL, Advanced level HDL Coding.
- ❖ All VLSI design methodologies should be covered during Laboratory sessions.
- ❖ One small Project per group of 2/3 students should be given as part of laboratory work

REFERENCE BOOKS:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo kang, Yusuf Leblebici, Third Edition. (TMH)
2. Basic VLSI Design By Puck Nell & Eshraghian, PHI, 3rd Ed.
3. Introduction to VLSI Systems by Mead C & Conway, Addison Wesley
4. Digital Integrated Circuits: A Design Perspective By Jan M. Rabaey, PHI
5. VHDL primer by J.Bhaskar, Addison Wesley, Pearson Ed.
6. VHDL by Douglas Perry (TMH)