

HEMCHANDRACHARYA NORTH GUJARAT UNIVERSITY, PATAN

B. E. COMPUTER ENGINEERING

B. E SEMESTER – III (CE)

(Effective From June 2006)

CE 303: COMPUTER SYSTEM ARCHITECTURE - I

TEACHING SCHEME:

THEORY 03 HRS/WEEK

PRACT 02 HRS/WEEK

TOTAL 05 HRS/WEEK

EXAM SCHEME:

THEORY 100 MARKS(3 HRS)

PRACT 25 MARKS

TW/VIVA 25 MARKS

TOTAL 150 MARKS
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UNIT - I

Concept of Von Newman Machine, components in a computer, functions of various of components, bus structure, arithmetic logic unit, computer arithmetic: addition/subtraction of integers, multiplication and division of integers; floating point arithmetic operations, BCD arithmetic operations.

UNIT - II

Concept of instruction format and instruction set of a computer, types of operands and operations; addressing modes; processor organization, register organization and stack organization; instruction cycle; basic details of Pentium processor and power PC processor, RISC and CISC instruction set.

UNIT - III

Memory devices: Semiconductor and ferrite core memory, main memory, cache memory, associative memory organization; concept of virtual memory; memory organization and mapping; partitioning, demand paging, segmentation; magnetic disk organization, introduction to magnetic tape and CDROM.

UNIT - IV

IO Devices: Programmed IO, interrupt driver IO, DMA, IO modules, IO addressing; IO channel, IO Processor, Dot matrix printer, ink jet printer, laser printer.

UNIT - V

Advanced concepts: Horizontal and vertical instruction format, microprogramming, microinstruction sequencing and control; instruction pipeline; parallel processing; problems in parallel processing; data hazard, control hazard.

REFERENCE BOOKS:

1. "Computer organization and architecture", Williams Stallings, PHI of India, 1998.
2. Computer organization, Carl Hamachar, Zvonko Vranesic and Safwat Zaky, McGraw Hill International Edition.
3. Computer Architecture & Organization, John P. Hayes, TMH III Edition.